

## SELECTABLE 6 DECADE CMOS DIVIDER

August 2007

### FEATURES:

- Selectable Divide by  $10^1$ ,  $10^2$ ,  $10^3$ ,  $10^4$ ,  $10^5$  or  $10^6$
  - Clock Input Shaping Network Accepts Fast or Slow Edge Inputs
  - Active Oscillator Network for External Crystal
  - Square Wave Output
  - Output TTL Compatible at +4.5V Operation
  - High Noise Immunity
  - Reset
  - All Inputs Protected
  - +3V to +15V Operation ( $V_{DD} - V_{SS}$ )
  - Low Power Dissipation
  - RDD106 (DIP); RDD106-S (SOIC)
- See Figure 1 -

### PIN ASSIGNMENT - TOP VIEW

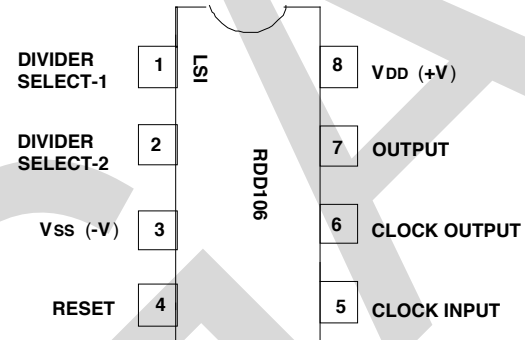


FIGURE 1

### MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	TSTG	-65 to +150	°C
Operating Temperature	TA	-40 to +85	°C
DC Supply Voltage ( $V_{DD} - V_{SS}$ )		+18	V
Voltage at any input	$V_{IN}$	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V

### DESCRIPTION OF OPERATION:

The RDD106 is a CMOS six decade divider circuit that advances on each negative transition of the input clock pulse. When the reset input is high the circuit is cleared to zero. The clock input is applied to a single stage inverting amplifier network whose output is brought out so that an external crystal network can be used to form an oscillator circuit. If the clock output is not used, the amplifier acts as an input buffer. Two select inputs are provided which enables the circuit to divide by  $10^1$ ,  $10^2$ ,  $10^3$ ,  $10^4$ ,  $10^5$  or  $10^6$ .

The Output Division is selected according to the following truth table:

DIVIDER SELECT INPUTS:		OUTPUT
SELECT 2	SELECT 1	DIVISION
*1	*F	1,000,000
*0	*F	100,000
0	0	10,000
0	1	1,000
1	0	100
1	1	10

\*Note: Not valid below 4.5V. F = Floating

### DC ELECTRICAL CHARACTERISTICS:

(All voltages referenced to  $V_{SS}$ )

	$V_{DD}$	-40°C	+25°C	+85°C	UNIT	
Quiescent Current (Pin 1 = $V_{DD}$ )	4.5V	2.0	1.5	1.0	$\mu A$ Max	
	10V	3.0	2.5	2.0	$\mu A$ Max	
Quiescent Current (Pin 1 = F)	4.5V	4.5	3.0	2.5	$\mu A$ Max	
	10V	25	18	15	$\mu A$ Max	
Quiescent Current (Pin 1 = $V_{SS}$ )	4.5V	11	8.0	6.0	$\mu A$ Max	
	10V	50	39	30	$\mu A$ Max	
Output Voltage, Low Level	4.5V	0.01	0.01	0.05	V Min	
	10V	0.01	0.01	0.05	V Min	
	High Level	4.5V	4.49	4.49	4.45	V Max
		10V	9.99	9.99	9.95	V Max
Pin1 Sink / Source Current (Pin 1 = $V_{SS} / V_{DD}$ )	4.5V	8	6	5	$\mu A$ Max	
	10V	46	36	29	$\mu A$ Max	
Input Noise Immunity (Low and High)	4.5V	1.3	1.3	1.3	V Min	
	10V	3.0	3.0	3.0	V Min	

### Output Drive Current:

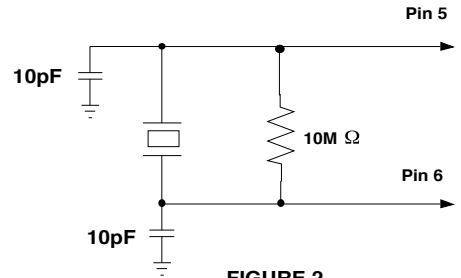
N-Channel Sink Current ( $V_{OUT} = V_{SS} + 0.4V$ )	4.5V	2.5	2.0	1.5	mA Min
	10V	7.0	5.5	4.0	mA Min
P-Channel Source Current ( $V_{OUT} = V_{DD} - 1V$ )	4.5V	3.0	2.5	1.8	mA Min
	10V	7.7	6.0	4.5	mA Min
Input Capacitance (any input)	-	5.0	-	-	pF Max

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

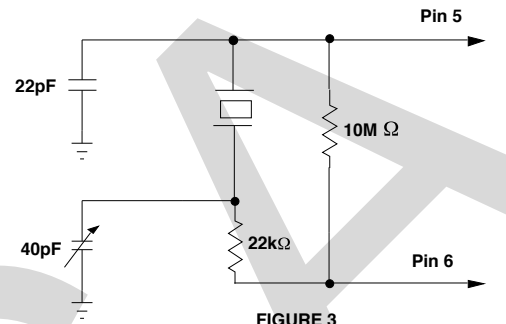
### DYNAMIC ELECTRICAL CHARACTERISTICS:

( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

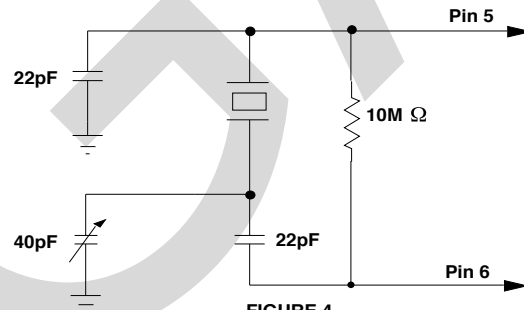
	V <sub>DD</sub>	MIN	MAX	UNIT	
Clock Input Frequency	3.0V	0	5	MHz	
	4.5V	0	10	MHz	
	10V	0	20	MHz	
	15V	0	30	MHz	
Clock Output Propagation Delay, C <sub>L</sub> = 15pF	4.5V	-	30	ns	
	10V	-	15	ns	
Output Rise & Fall Times	4.5V	-	40	ns	
	10V	-	20	ns	
Propagation Delay to Output (per decade)	4.5V	-	160	ns	
	10V	-	75	ns	
Reset Pulse Width	4.5V	160	-	ns	
	10V	75	-	ns	
Reset Removal Time	4.5V	-	160	ns	
	10V	-	75	ns	
Reset Propagation Delay to Output	4.5V	-	200	ns	
	10V	-	100	ns	
Select Input Setup Time	4.5V	-	100	ns	
	10V	-	50	ns	
Dynamic V <sub>DD</sub> Current	<b>Freq</b>				
	5MHz	3.0V	-	0.3	mA
	10MHz	4.5V	-	1.0	mA
	20MHz	10V	-	6.5	mA
30MHz	15V	-	17	mA	



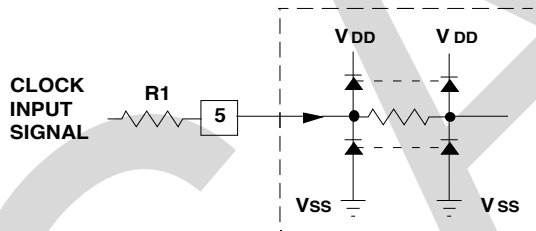
**FIGURE 2**  
TYPICAL OSCILLATOR CIRCUIT - 10MHz TO 30MHz



**FIGURE 3**  
TYPICAL OSCILLATOR CIRCUIT WITH TRIM - 2MHz AND BELOW

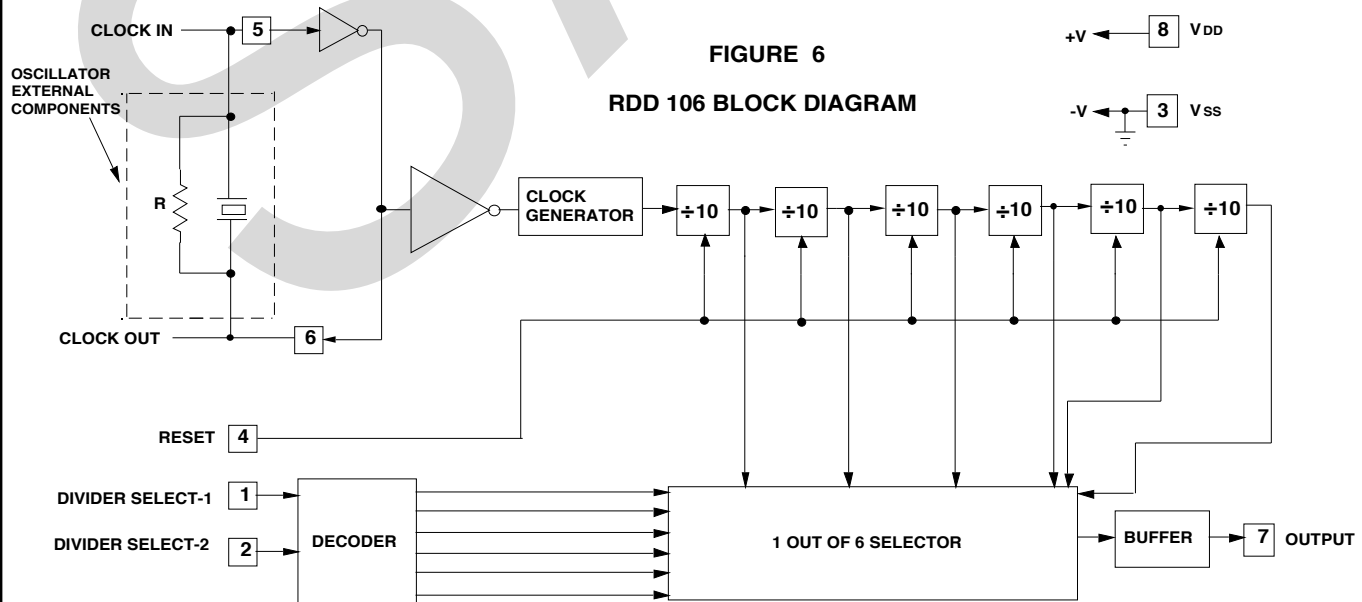


**FIGURE 4**  
TYPICAL OSCILLATOR CIRCUIT WITH TRIM - 2MHz TO 10MHz



**FIGURE 5. TYPICAL INPUT**

If input signals are less than  $V_{SS}$  or greater than  $V_{DD}$ , a series input resistor,  $R_1$ , should be used to limit the maximum input current to 2mA.



**FIGURE 6**

**RDD 106 BLOCK DIAGRAM**