LSI/CSI

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (631) 271-0400 FAX (631) 271-0405

LS7210

PROGRAMMABLE DIGITAL DELAY TIMER

June 2006

FEATURES:
- Programmable Delay from 6ms to "Infinity"
- Can be Cascaded for Sequential Events or Extended Delay
- +4.75V to +15V Operation (Vss - VDD)
- On Chip Oscillator or External Clock time base
- High Noise Immunity
- LS7210 (DIP); LS7210-S (SOIC) - (See Figure 1)

DESCRIPTION:
The LS7210 is a MOS programmable digital timer that can generate a delay in the range of 6ms to infinity. The delay is programmed by 5 binary weighted input bits in combination with the time base provided. The chip can be operated in four different modes: Delayed Operate, Delayed Release, Dual Delay and One Shot. These modes are selected by the control inputs A and B.

INPUT/OUTPUT DESCRIPTION:
OSCILLATOR Input (Pin 5)
The frequency of the internal oscillator is set by an RC network connected to the OSC input, as shown in Figure 2. The nominal oscillator frequency, f, at room temperature is given by f ≈ 1/RC where R values range from a minimum of 47KΩ to a maximum 3MΩ.
NOTE: Oscillation accuracy from chip to chip for a fixed value of RC, is ± 10%. (Parts can supplied to tighter tolerances.)

EXTERNAL CLOCK Input (Pin 6)
If the internal oscillator is not used, the chip can be driven by an external clock applied to this input.

CLOCK SELECT Input (Pin 4)
The internal oscillator or the external clock is selected by the proper logic level applied to this input. A logic 1 selects the external clock and logic 0 selects the internal oscillator. (See Note 1)

TRIGGER Input (Pin 3)
A positive or a negative transition at the trigger input initiates a delay in turning on or off the output. A negative transition always turns on the output with or without delay depending on the selected mode. A positive transition at the trigger input always turns off the output (with the exception of one-shot mode) with or without delay depending on the selected mode. The delay is a function of the time base frequency and the weighting factor programmed at the weighting bit inputs. The trigger input is clocked into the input latch with the negative edge of the selected time base clock. All timings begin after the latch has been set up. (See Note 1)

WEIGHTING FACTOR Inputs, $\overline{WB0}$-$\overline{WB4}$ (Pins 12-8)
A delay from the trigger input to the output is programmed by applying 1's complement binary weighted numbers at these 5 inputs. (See Note 1) The exact equation for the delay is:

$$\textbf{Delay} = \frac{(1 + 1,023N)}{f}$$

f = Oscillation Frequency
N = Weighting Factor

PIN ASSIGNMENT - TOP VIEW

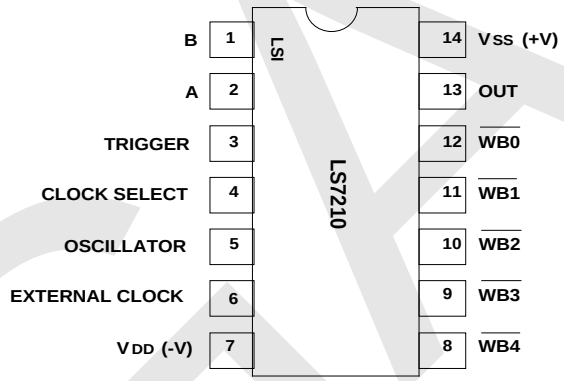


FIGURE 1

TABLE 1. WEIGHTING BITS ASSIGNMENTS

INPUTS	VALUE
$\overline{WB0}$	1
$\overline{WB1}$	2
$\overline{WB2}$	4
$\overline{WB3}$	8
$\overline{WB4}$	16

Example: For a weighting factor of 25, inputs $\overline{WB4}$, $\overline{WB3}$, and $\overline{WB0}$ should be programmed to logic 0.

MODE SELECT Inputs A, B (Pins 2, 1)
The chip can be programmed to operate in four different modes by applying the logic levels to inputs A and B as indicated in Table 2. The mode select inputs are clocked into the input latches with the negative edge of the time base clock. These inputs should not be changed while a delay timing is in progress. (See Note 1)

TABLE 2. MODE SELECTION

CONTROL A	CONTROL B	MODE
1	1	Dual Delay
1	0	Delayed Release
0	1	Delayed Operate
0	0	One Shot

OUT Output (Pin 13)
The output is an open drain FET. To obtain proper switching of the output between Logic 0 and 1 levels, an external pull down resistor to VDD must be used. If the output is used only as a current source, no such pull down is needed. The output is logically inverted with respect to the trigger input.

VSS, VDD (Pins 14, 9)
Supply voltage positive, negative terminals.

NOTE 1: These inputs have internal pullup resistors.

MODE DEFINITION TIMING DIAGRAM: (See Figure 3)

DUAL DELAY MODE
Thls is the Default Mode when the inputs A and B are left unprogrammed. The function of the Dual Delay mode is to provide a time delay on both the turn-on and turn-off of the output. Once turned on, the output will remain on as long as the trigger input is Logic 0. Once turned off, the output will remain off as long as the trigger input is a logic 1.

DELAYED OPERATE MODE
This mode causes a retriggerable delay in turning the output on in response to a negative edge at the trigger input. The output is turned off without delay in response to a positive transition at the trigger input.

DELAYED RELEASE MODE
This mode causes a retriggerable delay in turning off the output whenever there is a positive transition at the trigger input. The output is turned on without delay in response to a negative transition at the trigger input.

ONE-SHOT MODE
In this mode, the chip functions like a retriggerable monostable multi-vibrator. The output is turned on whenever there is a negative transition at the trigger input. At the end of the programmed delay, the output is turned off automatically. If there is a negative transition at the trigger input before the delay is over, the delay is restarted. A positive transition at the trigger input has no effect on the output in this mode. **NOTE**: In One-Shot mode, the TRIGGER input must be held at logic 1 during a power-up.

ABSOLUTE MAXIMUM RATINGS: (All voltages referenced to V_{DD})

	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{SS}	+18	V
Voltage (Any Pin)	V_{IN}	0 to V_{SS} + 0.3	V
Operating Temperature	T_A	-25 to +70	°C
Storage Temperature	T_{STG}	-65 to +150	°C

DC ELECTRICAL CHARACERISTICS:
(-25°C ≤ T_A ≤ +70°C unless otherwise specified. All voltages referenced to V_{DD})

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
Suppy Voltage	V_{SS}	+4.75	+15.0	V	
Supply Current	I_{SS}	-	3.0	mA	V_{SS} = +15V, output off
Trigger Input					
Logic 1	V_{TH}	V_{SS} - 1	V_{SS}	V	-
Logic 0	V_{TL}	0	0.2V_{SS}	V	-
All Other Inputs					
Logic 1	V_{IH}	0.8V_{SS}	V_{SS}	V	-
Logic 0	V_{IL}	0	0.2V_{SS}	V	-
Output					
Source Current	Io	+1.0	-	mA	V_{SS} = + 5V
for Vo = Vss - 1V	Io	+2.8	-	mA	V_{SS} = +10V
	Io	+4.2	-	mA	V_{SS} = +15V

SWITCHING CHARACTERISTICS: (See Figure 4)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Oscillator Frequency	f_{OSC}	-	50	kHz
External Clock Frequency	f_{ext}	DC	160	kHz
External Clock, Positive Pulse Width	t_H	3	-	µs
External Clock, Negative Pulse Width	t_L	3	-	µs
A, B and Trigger Input Set-Up Time	t_S	-	300	ns
Time-base Clock to Output Delay (turn-on delay in Delayed Release mode and turn-off delay in Delayed Operate mode)	t_{nd}	-	1	µs
Time-base Clock to Output Delay at the End of Time Out	t_{od}	-	1.6	µs
Time-base Clock to Output Delay (turn-on delay in One- Shot Mode)	t_{sd}	-	600	ns

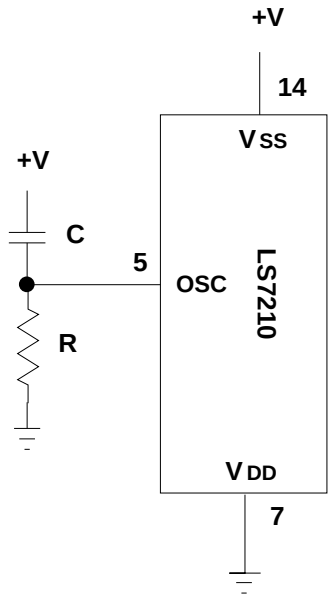


FIGURE 2.

LS7210 OSCILLATOR CONNECTION

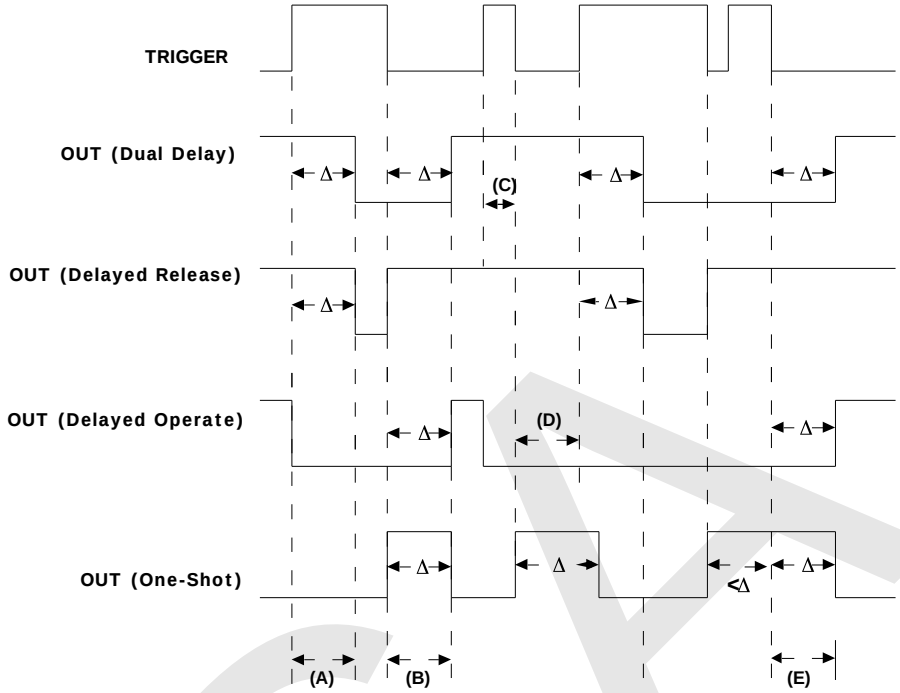


FIGURE 3. MODE DEFINITION TIMING DIAGRAM

A - Turn-off delay in Dual Delay and Delayed Release mode.

B - Turn-on delay in Dual Delay and Delayed Operate mode; one-shot period in One-Shot mode.

C - Output remains on in Delayed Release and Dual Delay modes due to negative trigger transition before the turn-off delay is over.

D - Output remains off in Delayed Operate mode due to positive trigger transition before the turn-on delay is over.

E - One-Shot period extended by re-triggering.

Note: Δ is the programmed delay.

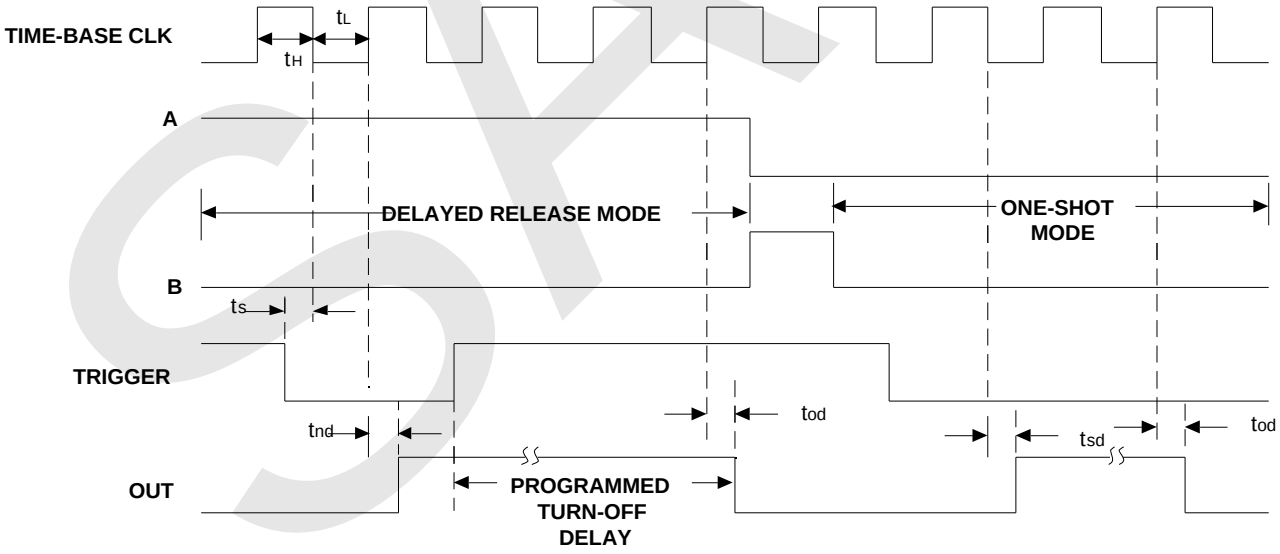


FIGURE 4. LS7210 TIMING DIAGRAM

Note 1. - A, B and Trigger inputs are clocked into the input latches with the negative edge of the time-base cloc

Note 2. - In all modes except One-Shot, the output changes with the positive transition of the time-base clock. In One-Shot mode the output is turned on with the negative transition and turned off with the positive transition of the time-base clock.

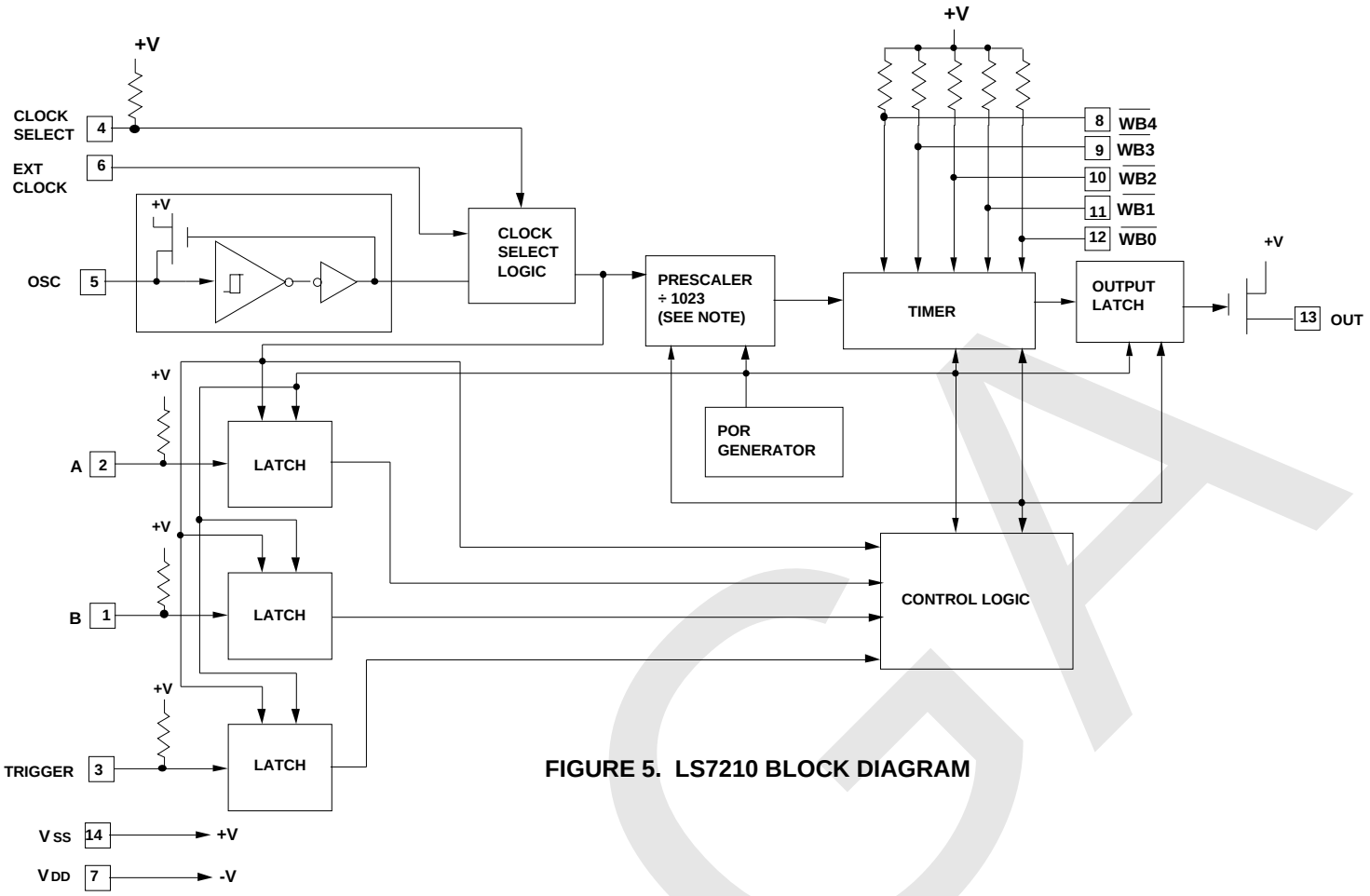
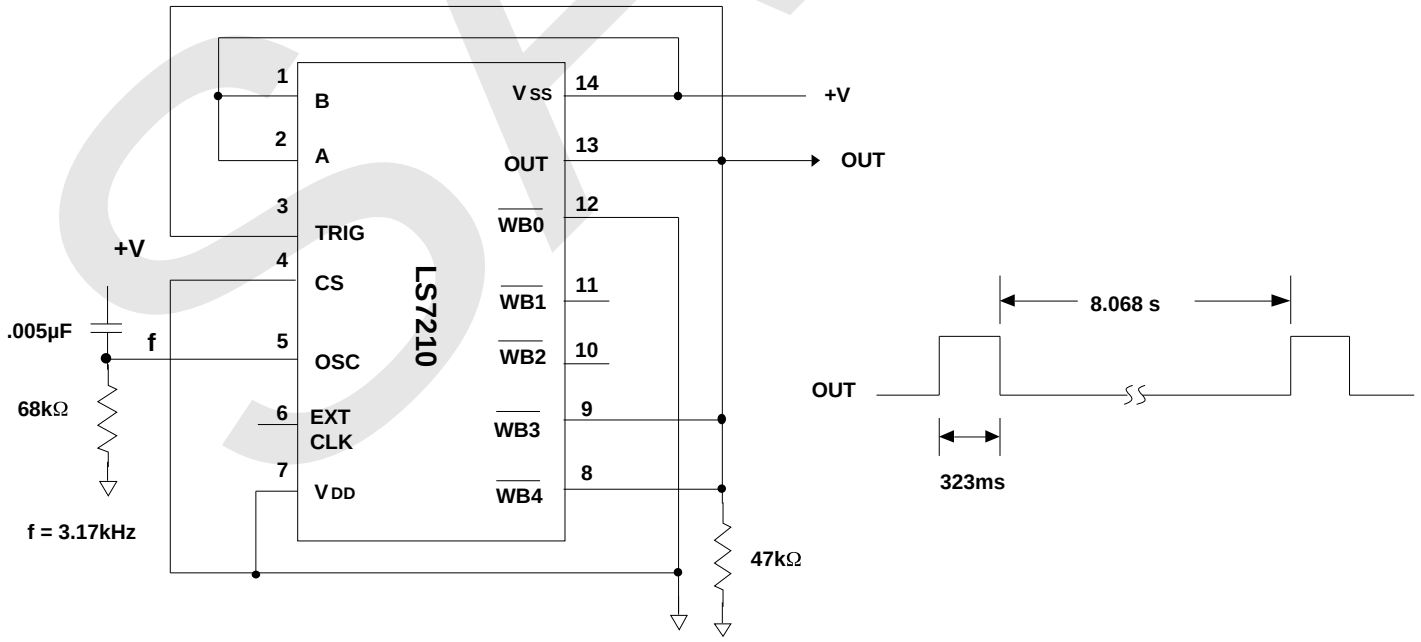


FIGURE 5. LS7210 BLOCK DIAGRAM

NOTE: ÷ 1023 is standard. Any number from 1 to 1022 can be mask programmed.

FIGURE 6. ASYMMETRICAL FLASHER



NOTE: Inputs A, B in Dual-Delay mode. For symmetical flasher tie Pins 8, 9, 10, 11 and 12 to fixed logic level.