

PROGRAMMABLE DIGITAL DELAY TIMER

FEATURES:

- 8-bit programmable delay from microseconds to days
- On chip oscillator (RC or Crystal) or external clock time base
- Selectable prescaler for real time delay generation based on 50Hz/60Hz time base or 32,768Hz watch crystal
- Four operating modes
- Reset input for delay abort
- Low quiescent and operating current
- Direct relay drive
- +3V to +18V operation (VDD - VSS)
- **LS7211N, LS7212N (DIP); LS7211N-S, LS7212N-S (SOIC)**

- See Figure 1 -

DESCRIPTION:

The **LS7211N** and **LS7212N** are CMOS integrated circuits for generating digitally programmable delays. The delay is controlled by 8 binary weighted inputs, WB0 - WB7, in conjunction with an applied clock or oscillator frequency. The programmed time delay manifests itself in the Delay Output (OUT) as a function of the Operating Mode selected by the Mode Select inputs A and B: One-Shot, Delayed Operate, Delayed Release or Dual Delay. The time delay is initiated by a transition of the Trigger Input (TRIG).

I/O DESCRIPTION:

MODE SELECT Inputs A & B (Pins 1 & 2)

The 4 operating modes are selected by Inputs A and B according to Table 1

TABLE 1. MODE SELECTION

A	B	MODE
0	0	One-Shot (OS)
0	1	Delayed Operate (DO)
1	0	Delayed Release (DR)
1	1	Dual Delay (DD)

Each input has an internal pull-up resistor of about 500k .

One-Shot Mode (OS)

A positive transition at the TRIG input causes OUT to switch low without delay and starts the delay timer. At the end of the programmed delay timeout, OUT switches high. If a delay timeout is in progress when a positive transition occurs at the TRIG input, the delay timer will be restarted. A negative transition at the TRIG input has no effect.

Delayed Operate Mode (DO)

A positive transition at the TRIG input starts the delay timer. At the end of the delay timeout, OUT switches low. A negative transition at the TRIG input causes OUT to switch high without delay. OUT is high when TRIG is low.

PIN ASSIGNMENT - TOP VIEW

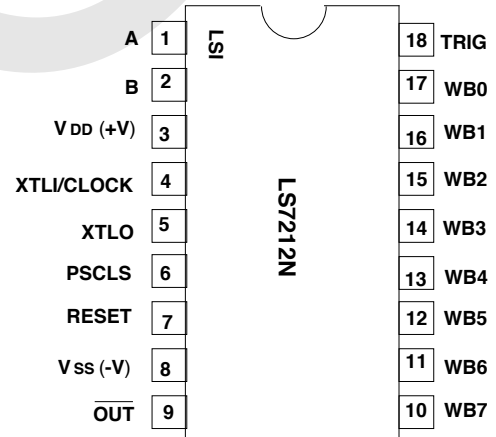
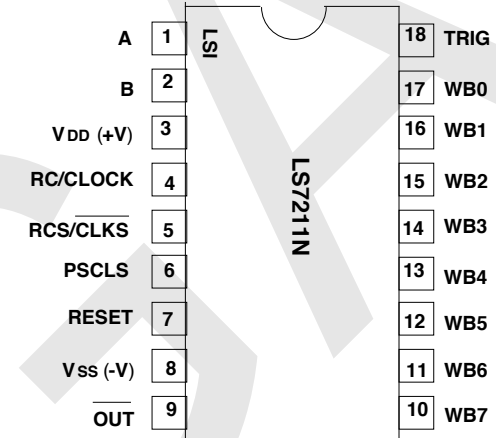


FIGURE 1

Delayed Release Mode (DR)

A negative transition at the TRIG input starts the delay timer. At the end of the delay timeout, OUT switches high. A positive transition at the TRIG input causes OUT to switch low without delay. OUT is low when TRIG is high.

Dual Delay Mode (DD)

A positive or negative transition at the TRIG input starts the delay timer. At the end of the delay timeout, OUT switches to the logic state which is the inverse of the TRIG input. If a delay timeout is in progress when a transition occurs at the TRIG input, the delay timer is restarted.

TRIGGER Input (TRIG, Pin 18)

A transition at the TRIG input causes $\overline{\text{OUT}}$ to switch with or without delay, depending on the selected mode. The TRIG input to $\overline{\text{OUT}}$ transition relation is always opposite in polarity, with the exception of One-Shot mode. (See Mode definitions above.) TRIG input has an internal pull-down resistor of about 500k and is buffered by a Schmitt trigger to provide input hysteresis.

LS7211N TIME BASE Input (RC/CLOCK, Pin 4)

For **LS7211N**, the basic timing signal is applied at the RC/CLOCK input. The clock can be provided from either an external source or generated by an internal oscillator by connecting an R-C network to this input.

The frequency of oscillation is given by $f \approx 1/RC$. Chip-to-chip oscillation tolerance is $\pm 5\%$ for a fixed value of RC.

The minimum resistance, R_{MIN} = 4000 , $V_{\text{DD}} = +4\text{V}$
 = 1200 , $V_{\text{DD}} = +10\text{V}$
 = 600 , $V_{\text{DD}} = +18\text{V}$

The external clock mode is selected by applying a logic low to the RCS/CLKS input (Pin 5); the internal oscillator mode is selected by applying a high level to the RCS/CLKS input.

LS7212N TIME BASE Input (XTLI/CLOCK, Pin 4)

For **LS7212N**, the basic timing clock is applied to the XTLI/CLOCK input from either an external clock source or generated by an internal crystal oscillator by connecting a crystal between XTLI/CLOCK input and the XTLO output (Pin 5).

LS7211N TIME BASE SELECT Input (RCS/CLKS, Pin 5)

For **LS7211N**, the external clock operation at Pin 4 is selected by applying a logic low to the RCS/CLKS input. The internal oscillator option with RC timer at Pin 4 is selected by applying a logic high at the RCS/CLKS input. RCS/CLKS input has an internal pull-down resistor of about 500k .

LS7212N TIME BASE Output (XTLO, Pin 5)

For **LS7212N**, when a crystal is used for generating the time base oscillation, the crystal is connected between XTLI/CLOCK and XTLO pins.

PRESCALER SELECT Input (PSCLS, Pin 6)

The PSCLS input is a 3-state input, which selects one of three prescale factors according to Table 2.

TABLE 2. PRESCALE FACTOR SELECTION

PSCLS Input Logic Level	S (Prescale Factor)	
	LS7211N	LS7212N
Float	1	1
VSS	3,000	32,768
VDD	3,600	32,768x60

Using prescale factors of 3000 and 3600, delays in units of minutes can be produced from 50Hz and 60Hz line sources. Prescale factors of 32,768 and 32,768 x 60 can be used to generate accurate delays in units of seconds and minutes, respectively, from a 32kHz watch crystal.

TIMER RESET Input (RESET, Pin 7)

When RESET input switches high, any timeout in progress is aborted and $\overline{\text{OUT}}$ switches high without delay. With RESET high, $\overline{\text{OUT}}$ remains high. When RESET switches low with TRIG low in any mode, $\overline{\text{OUT}}$ remains high. When RESET switches low with TRIG high in Delayed Operate and Dual Delay modes, the delay timer is started and $\overline{\text{OUT}}$ switches low at the end of the delay timeout. When RESET switches low with TRIG high in Delayed Release mode, $\overline{\text{OUT}}$ switches low without delay. When RESET switches low with TRIG high in One-Shot mode, $\overline{\text{OUT}}$ remains high. RESET input has an internal pull-down resistor of about 500k , and is buffered by a Schmitt Trigger to provide input hysteresis.

VSS (-V, Pin 8)

Supply voltage negative terminal or GND.

DELAY Output ($\overline{\text{OUT}}$, Pin 9)

Except in One-Shot mode, $\overline{\text{OUT}}$ switches with or without delay (depending on mode) in inverse relation to the logic level of the TRIG input. In One-Shot mode, a timed low level is produced at $\overline{\text{OUT}}$, in response to a positive transition of the TRIG input.

WEIGHTING BIT Inputs (WB7 to WB0, Pins 10 - 17)

Inputs WB0 through WB7 are binary weighted delay bits used to program the delay according to the following relations:

$$\text{One-Shot Mode: Pulse width} = \frac{SW}{f}$$

$$\text{All other Modes: Delay} = \frac{SW + 0.5}{f}$$

Where:

S = Prescale factor (See Table 2)

f = Time base frequency at Pin 4

W = WB0 + WB1 + WB7

The weighting factor W is calculated by substituting in the equation above for W, the weighted values for all the WB inputs that are at logic high. The weighted values for the WB inputs are shown in Table 3. Each WB input has an internal pull-down resistor of about 500k .

TABLE 3. BIT WEIGHTS

BITS	VALUE
WB0	1
WB1	2
WB2	4
WB3	8
WB4	16
WB5	32
WB6	64
WB7	128

VDD (+V, Pin 3)

Supply voltage positive terminal.

ABSOLUTE MAXIMUM RATINGS: (All voltages referenced to Vss)

	SYMBOL	VALUE	UNIT
DC Supply Voltage	VDD	+19	V
Voltage (Any Pin)	VIN	Vss - 0.3 to VDD + 0.3	V
Operating Temperature	TA	-20 to +85	°C
Storage Temperature	TSTG	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Voltages referenced to Vss)

Characteristic	SYMBOL	VDD	-20°C		+25°C		+85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
Supply Voltage	VDD	-	3.0	18.0	3.0	18.0	3.0	18.0	V	-
Supply Current	IDD	3.0	-	66	-	55	-	44	µA	with the clock off and all inputs floating.
		10.0	-	252	-	210	-	168	µA	
		18.0	-	540	-	450	-	360	µA	
Input Voltages:										
Reset, Trigger Low	VTL	3.0	-	0.8	-	0.75	-	0.7	V	-
		10.0	-	2.3	-	2.2	-	2.1	V	
		18.0	-	3.9	-	3.8	-	3.7	V	
Reset, Trigger High	VTH	3.0	2.2	-	2.1	-	2.0	-	V	-
		10.0	6.1	-	6.0	-	5.9	-	V	
		18.0	9.7	-	10.5	-	11.0	-	V	
Reset, Trigger Hysteresis		3.0	0.7	-	0.7	-	0.7	-	V	-
		10.0	2.2	-	2.2	-	2.2	-	V	
		18.0	3.9	-	3.9	-	3.9	-	V	
All other inputs, Low	VIL	3.0	-	1.1	-	1.1	-	1.1	V	-
		10.0	-	4.5	-	4.5	-	4.5	V	
		18.0	-	10.6	-	10.6	-	10.6	V	
All other inputs, High	VIH	3.0	1.9	-	1.9	-	1.9	-	V	-
		10.0	6.5	-	6.5	-	6.5	-	V	
		18.0	13.3	-	13.3	-	13.3	-	V	
Input Currents:										
PSCLS Low	IPL	3.0	-	3.2	-	2.5	-	1.9	µA	Input at Vss
		10.0	-	31	-	24	-	18	µA	
		18.0	-	84	-	65	-	49	µA	
PSCLS High	IPH	3.0	-	9.8	-	7.5	-	5.8	µA	Input at VDD
		10.0	-	31	-	24	-	18.2	µA	
		18.0	-	85	-	65	-	49	µA	
A, B Low	IML	3.0	-	6.0	-	5.0	-	4.0	µA	Input at Vss
		10.0	-	59	-	48	-	38	µA	
		18.0	-	157	-	128	-	98	µA	
A, B High	IMH	-	-	100	-	100	-	200	nA	Input at VDD
All other inputs, Low	IIL	-	-	100	-	100	-	200	nA	Input at Vss
All other inputs, High	IIH	3.0	-	33	-	27	-	23	µA	Input at VDD
		10.0	-	120	-	105	-	81	µA	
		18.0	-	121	-	107	-	82	µA	
Output Current:										
OUT Sink	IOSNK	3.0	13.2	-	10.1	-	7.0	-	mA	Vo = +0.5V
		10.0	26	-	19.7	-	15	-	mA	
		18.0	30.7	-	23.6	-	17	-	mA	
OUT Source	IOSRC	3.0	4.1	-	3.2	-	2.1	-	mA	Vo = VDD - 0.5V
		10.0	7.2	-	5.5	-	4.1	-	mA	
		18.0	8.2	-	6.3	-	4.6	-	mA	

ELECTRICAL CHARACTERISTICS (Voltages referenced to Vss) (Con't)

Characteristic	SYMBOL	VDD	Min		Max		Min		Max		Unit	Condition
Switching Characteristics (See Fig. 3)												
RC Oscillator Frequency	fosc	3.0	-	1.8	-	1.4	-	1.05	MHz	-		
		10.0	-	4.5	-	3.4	-	2.6	MHz			
		18.0	-	8.0	-	4.0	-	3.0	MHz			
External Clock or Crystal Oscillator Frequency	fext	3.0	-	2.6	-	2.0	-	1.52	MHz	For prescale factor S = 32768 or 32768 x 60		
		10.0	-	5.3	-	4.0	-	3.0	MHz			
	fext	18.0	-	5.9	-	4.5	-	3.5	MHz	S = 1 or 3000 or 3600		
		3.0	-	7.2	-	5.5	-	4.2	MHz			
		10.0	-	16.0	-	12.8	-	9.7	MHz			
		18.0	-	15.9	-	13.0	-	9.1	MHz			
TRIG Set-Up Time	t1	-	39	-	50	-	66	-	ns	-		
A, B Set-Up Time	t2	-	0	-	0	-	0	-	ns			
WB0 - WB7 Set-Up Time	t3	-	0	-	0	-	0	-	ns			
Clock to Out Delay	t4	3.0	-	284	-	375	-	495	ns	CL = 50pF		
		10.0	-	98	-	130	-	172	ns			
		18.0	-	87	-	115	-	152	ns			

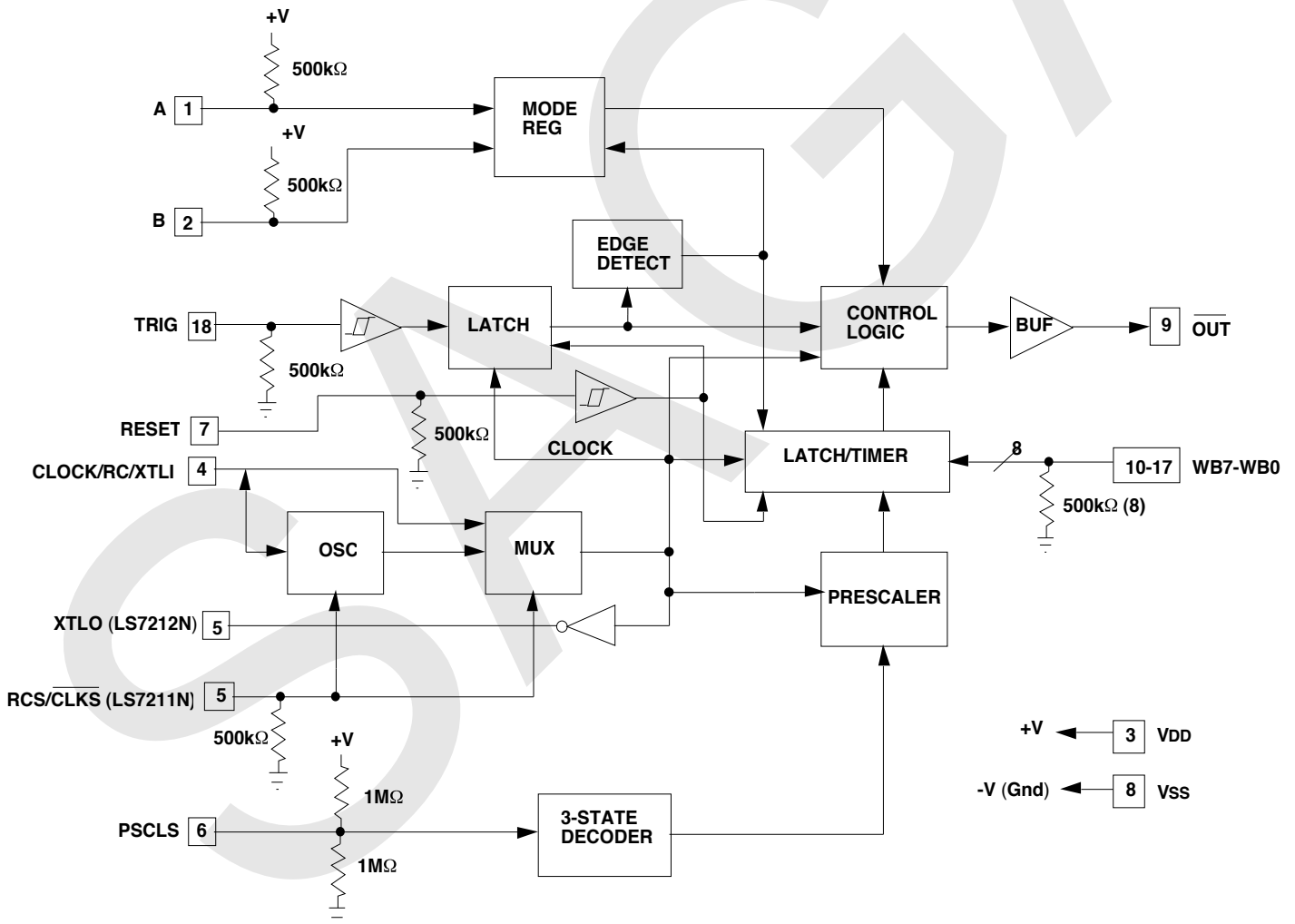
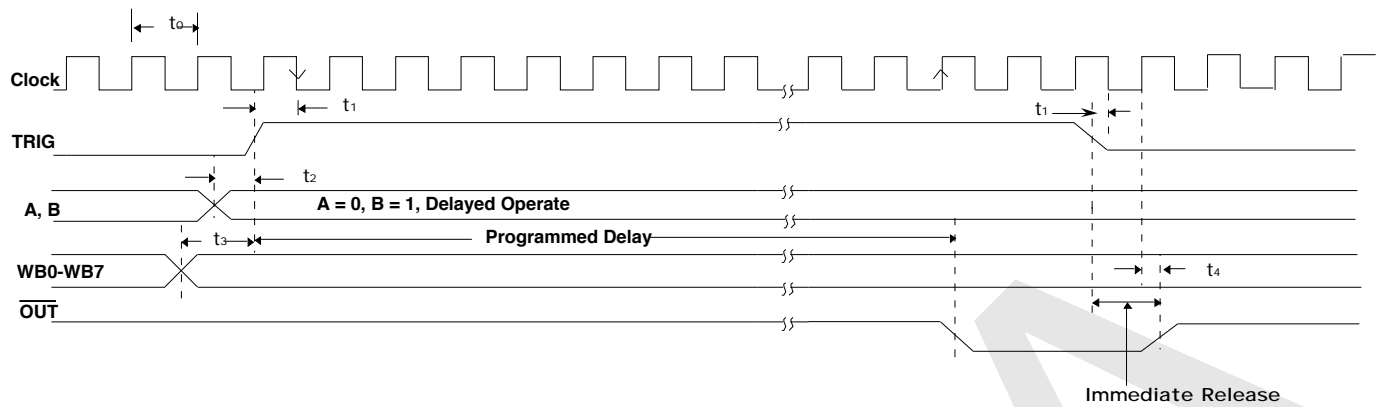


FIGURE 2. LS7211N / LS7212N BLOCK DIAGRAM

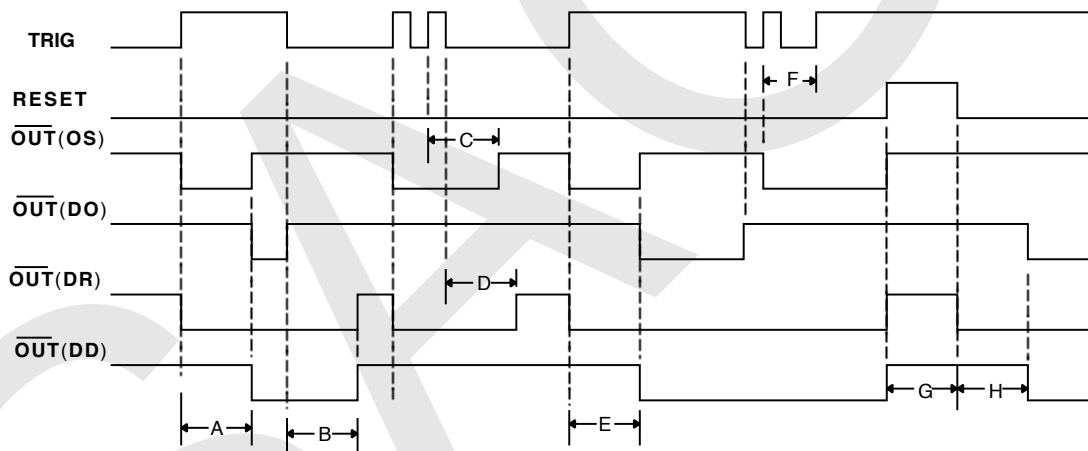


Note 1. TRIG input is clocked in by the negative edge of external clock.

Note 2. Inputs A, B and WB0 - WB7 are sampled only at a TRIG input transition and ignored at all other times.

Note 3. $\overline{\text{OUT}}$ is switched by the positive edge of the external clock.

FIGURE 3. INPUT/OUTPUT TIMING



A. Turn-on delay in DO and DD modes; Pulse-width in OS mode.

B. Turn-off delay in DR and DD modes.

C. Pulse-width extended by re-trigger in OS mode.

No effect in DO and DD modes because TRIG switches back low before turn-on delay has timed out.

D. Turn-off delay in DR mode.

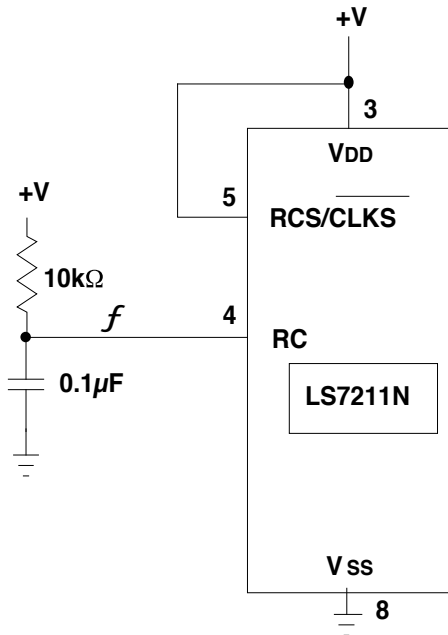
E. Turn-on delay in DO and DD modes; pulse-width in OS mode.

F. No effect in DO, DR and DD modes because of TRIG's switching back to opposite levels.

G. Time-outs aborted and $\overline{\text{OUT}}$ forces high by RESET.

H. After the removal of RESET, $\overline{\text{OUT}}$ switches to the inverse polarity of TRIG immediately (DR) or after the timeout (DO, DD). No effect in OS.

FIGURE 4. MODE ILLUSTRATION WITH TRIG, $\overline{\text{OUT}}$ AND RESET



$$f = \frac{1}{10 \times 10^3 \times 0.1 \times 10^{-6}} = 1\text{kHz}$$

FIGURE 5. RC- Oscillator Connection

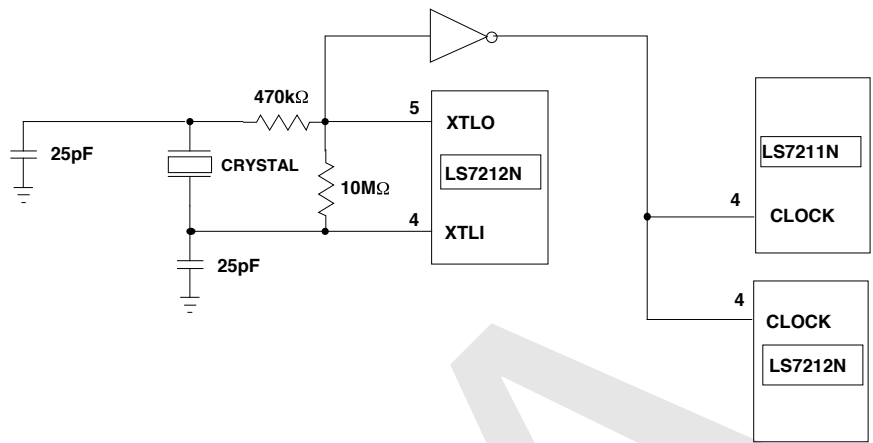


FIGURE 6. MULTI-TIMER WITH SINGLE CRYSTAL TIME-BASE

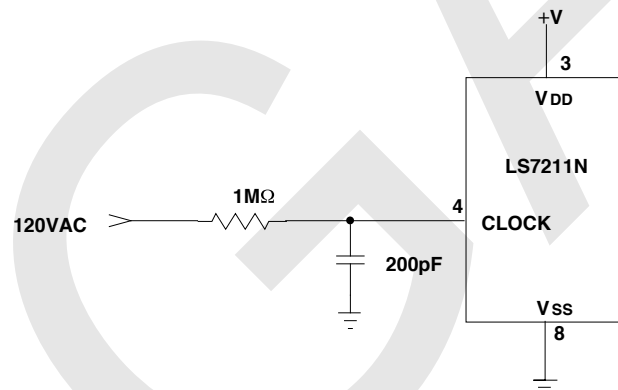
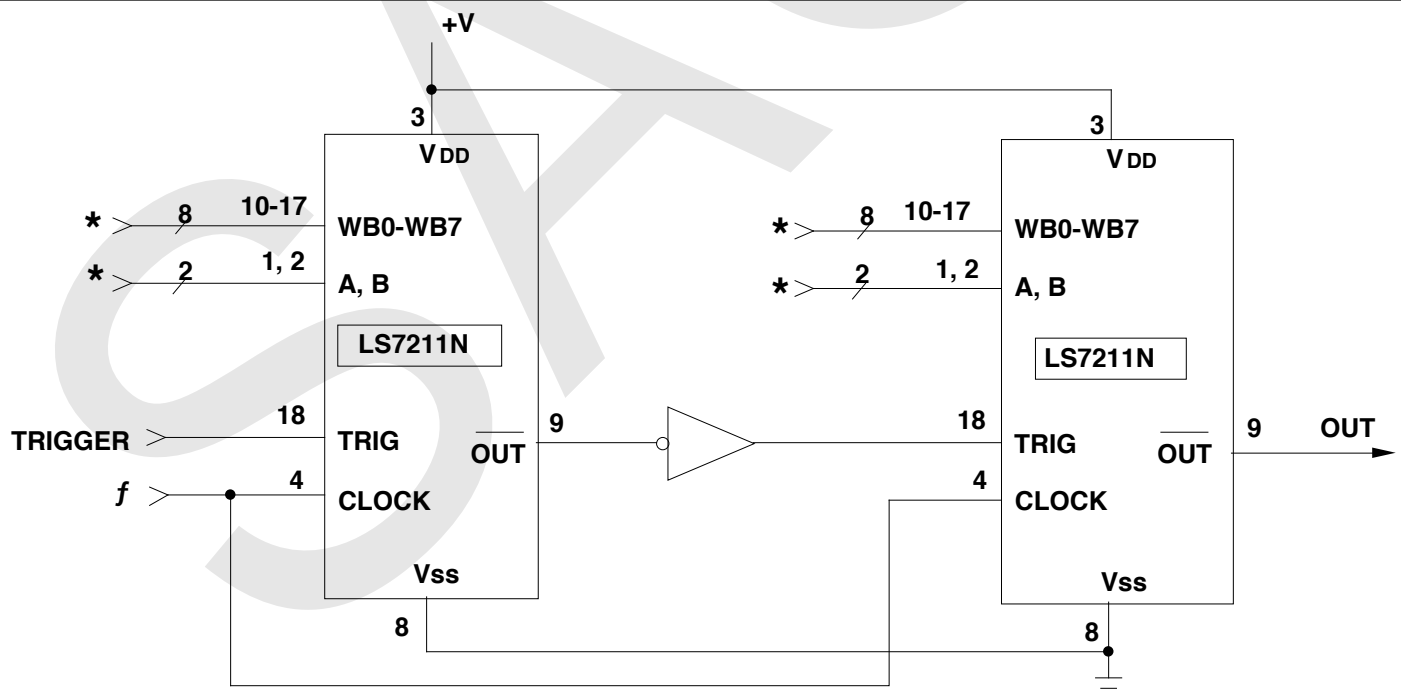
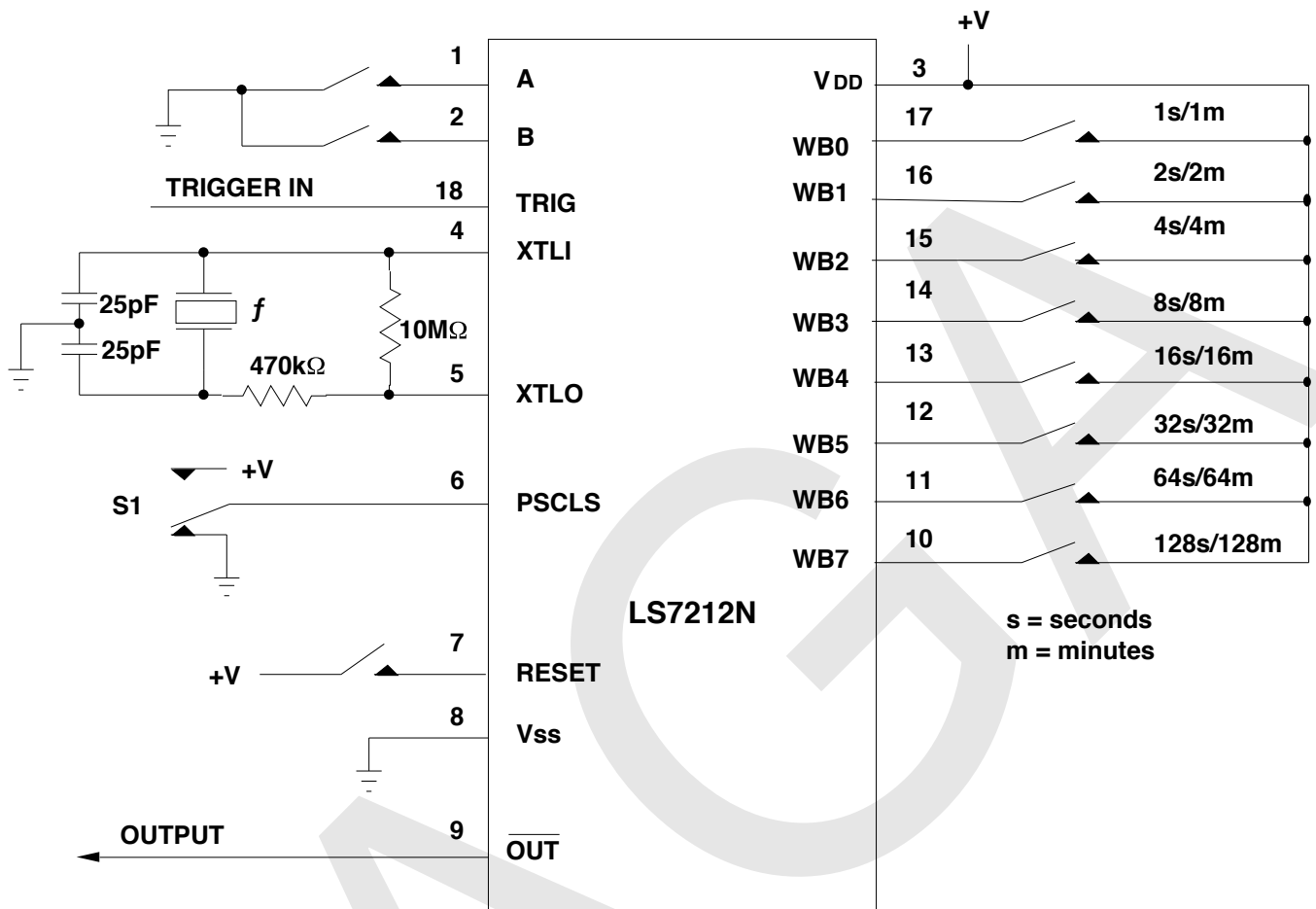


FIGURE 7. DRIVING CLOCK INPUT FROM THE AC LINE



* Connect for desired delay and mode

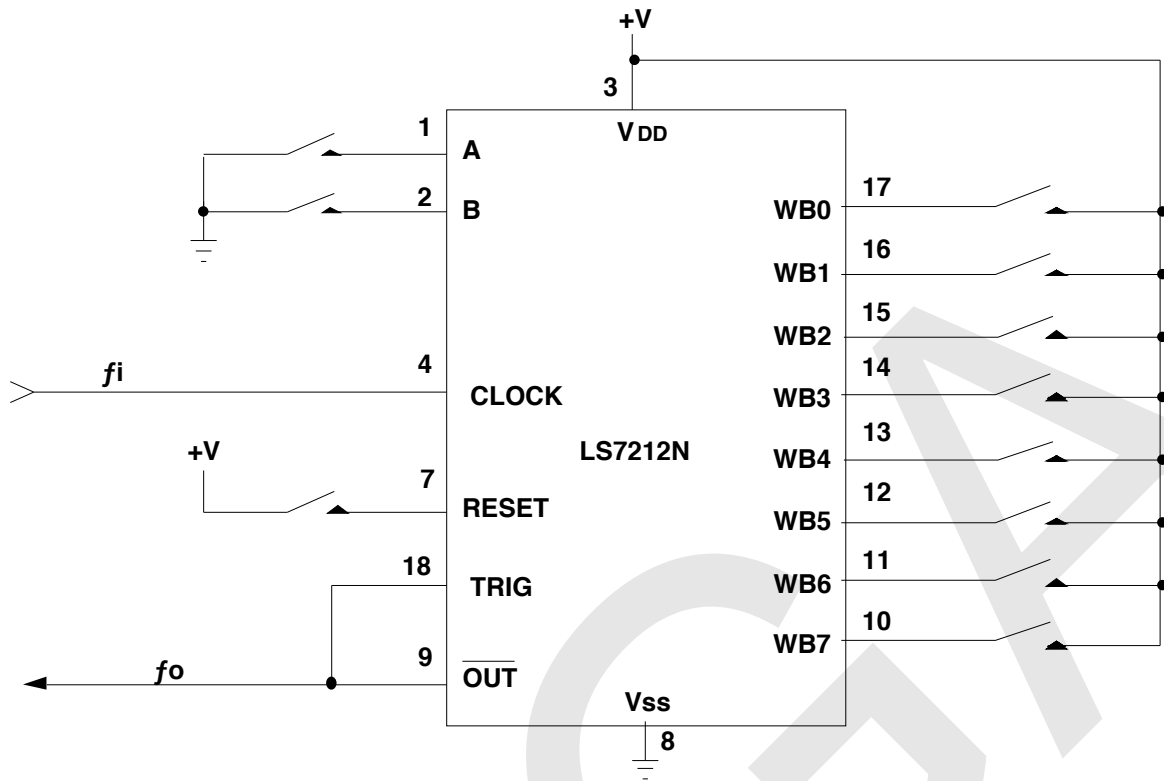
FIGURE 8. DELAY EXTENSION BY CASCADING



NOTE : Crystal Frequency, $f = 32,768\text{Hz}$
 Switch: S1 low: Delay increment = 1s; Maximum Delay = 255s
 S1 high: Delay increment = 1m; Maximum Delay = 255m

FIGURE 9. PROGRAMMABLE ACCURATE REAL-TIME DELAY GENERATION

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.



CASE 1. MODE = DO or DR; PRESCALE FACTOR, S = 1

In this setup a frequency division of the input clock, f_i by a factor of 2 to 257, in increments of 1 can be obtained according to the equation:

$$f_o = \frac{f_i}{W + 2} \quad \text{where } W \text{ (weighting factor) } = 0 \text{ to } 255$$

The f_o pulse width is non-symmetrical (non-50% duty -cycle)

CASE 2. MODE = DD; PRESCALE FACTOR, S = 1

In this setup a frequency division of the input clock, f_i by a factor of 2 to 512, in increments of 2 can be obtained according to the equation:

$$f_o = \frac{f_i}{2(W + 1)} \quad \text{where } W \text{ (weighting factor) } = 0 \text{ to } 255$$

The f_o pulse widths are symmetrical with 50% duty -cycle

EXAMPLES OF CASE 1 and CASE 2 FREQUENCY DIVISIONS WITH W = 2

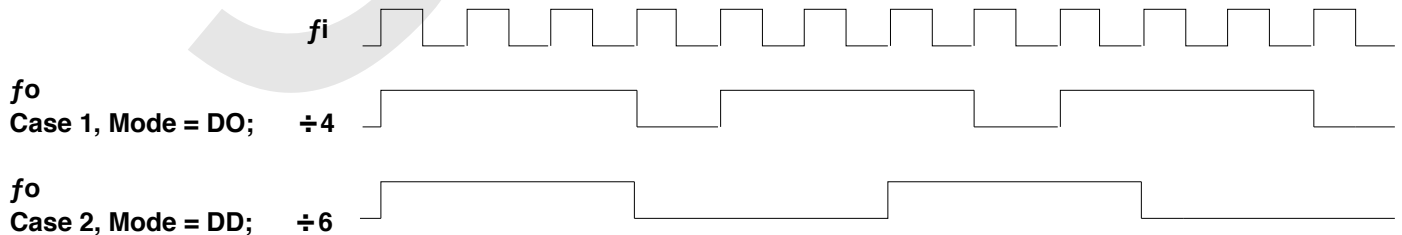


FIGURE 10. PROGRAMMABLE FREQUENCY DIVIDER