LSI/CSI

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LS7290

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STEPPER MOTOR CONTROLLER

FEATURES:

- Controls Bipolar and Unipolar motors
- Cost-effective replacement for L297
- Full, ½ step mode selected with mode input
- Direction control
- Reset input
- Step control input
- Enable input
- PWM chopper circuit for current control
- Two peak-current comparators with external reference input
- Step control frequency and duty cycle controlled by an external frequency source or by an internal crystal controlled oscillator (typically 8 MHz)
- All inputs and outputs TTL/CMOS compatible (TTL for 5V operation)
- 3V to 5.5V Operation (V_{DD} – V_{SS})
- LS7290 (DIP), LS7290-S (SOIC), LS7290-TS (TSSOP) – See Figure 1.

DESCRIPTION:

The LS7290 generates Phase Drive outputs and PWM outputs for controlling two-phase Bipolar Motors or four-phase Unipolar Motors, respectively. The LS7290 contains a mode controlled look-up table for generating the motor duty cycle drive sequences. There are four outputs which are used to drive two H-Bridges for the two motor windings in the Bipolar motor or the four driver transistors for the two center-tapped windings in the Unipolar motor (Refer to Table 2). The LS7290 can step a motor in full steps and half steps. The refresh rate is set using an internal oscillator controlled by a crystal or by use of an external input clock. Typical refresh rate is equal to 31.25kHz with the clock frequency set at 8MHz. Peak-current feedback control using pulse-width modulation is used in full-step or half-step modes. The chopper consists of a voltage comparator, flip-flop and external sense resistor. The internal oscillator sets the flip-flop and enables the $\overline{INH1}$ and $\overline{INH2}$ outputs at the beginning of each PWM cycle. Once the peak motor current causes the voltage across the sense resistors to reach the voltage set by VREF, the outputs are disabled until the next oscillator pulse. The VREF voltage sets the peak current in each motor winding.

INPUT/OUTPUT DESCRIPTION

$\overline{RESET}$ Input

Active low. Resets the PWM table pointer to HOME position per Table 2 and brings $\overline{INH1}$ and $\overline{INH2}$ low. Upon power-up, a POR circuit also resets the PWM table pointer.

$\overline{ENABLE}$ Input

Active low. When high (inactive), brings PHA, PHB, PHC, PHD, $\overline{INH1}$ and $\overline{INH2}$ outputs low.

$\overline{STEP}$ Input

Active low. A low-going pulse on this input causes the motor to advance one step.

PIN ASSIGNMENT
TOP VIEW

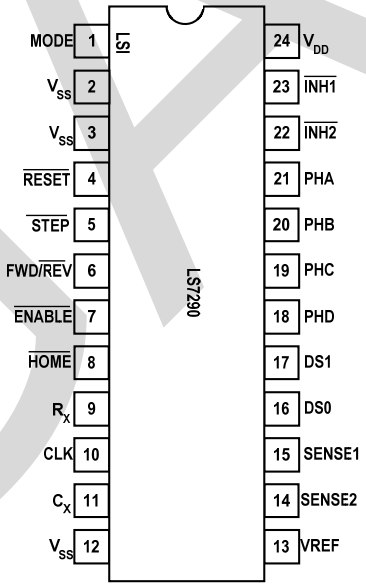


FIGURE 1.

NOTE: Pins 2 and 3 are used for factory test and must be tied to ground.

FRD/$\overline{RVRS}$ Input

A low input causes the motor to move in incremental steps in reverse direction per Table 2. A high input causes the motor to move in incremental steps in forward direction per Table 2. Switching directions can occur at any time.

MODE Input

Defines the stepping modes as follows:

	MODE
full step mode	0
½ step mode	1

Stepping mode can be changed at any time.

SENSE1 / SENSE2 Inputs

Inputs for motor winding current sense. A fractional-Ohm resistor connected in series with each of the H-Bridge drivers produce SENSE1 and SENSE2 voltages. These voltages are compared with VREF voltage input, for generating the PWM inhibit outputs.

VREF Input
External voltage reference for chopper circuit which determines the maximum motor winding current by regulating the PWM duty cycle. The SENSE resistors should satisfy the equations $R_{S1} = R_{S2} = V_{REF} / I_{MAX}$ where I_{MAX} is the maximum motor winding current.

R_X, C_X, CLK
These three pins can be configured in one of three ways to obtain the primary clock. A crystal connected between RX and CLK pins or a resistor-capacitor pair connected among all three pins (see Figure 4) can make use of the internal oscillator. Alternatively, the CLK pin can be driven from an external clock source.

DS0/DS1 Inputs
The phase drive is blanked out between steps by switching outputs $\overline{INH1}$ and $\overline{INH2}$ low in order to reduce audible noise and power consumption. The duration of the blanking is selected by DS0 and DS1 according to Table 1.

Table 1

DS1	DS0	Blanking Time, IPB, at f_c = 8Mz
0	0	1.25µs
0	1	2.50µs
1	0	3.75µs
1	1	5.00µs

PHA / PHB / PHC / PHD Outputs
The state of these phase outputs are determined by the look-up table and are used to control either the left or right half of each of the H-Bridge drivers. A low on a phase output enables the bottom driver while a high on the output enables the top driver.

$\overline{HOME}$ Output
Indicates Step0 state per Table 2 with a logic low.

$\overline{INH1}$ / $\overline{INH2}$ Outputs
These outputs are used to provide PWM control to each of the two H-Bridge drivers.

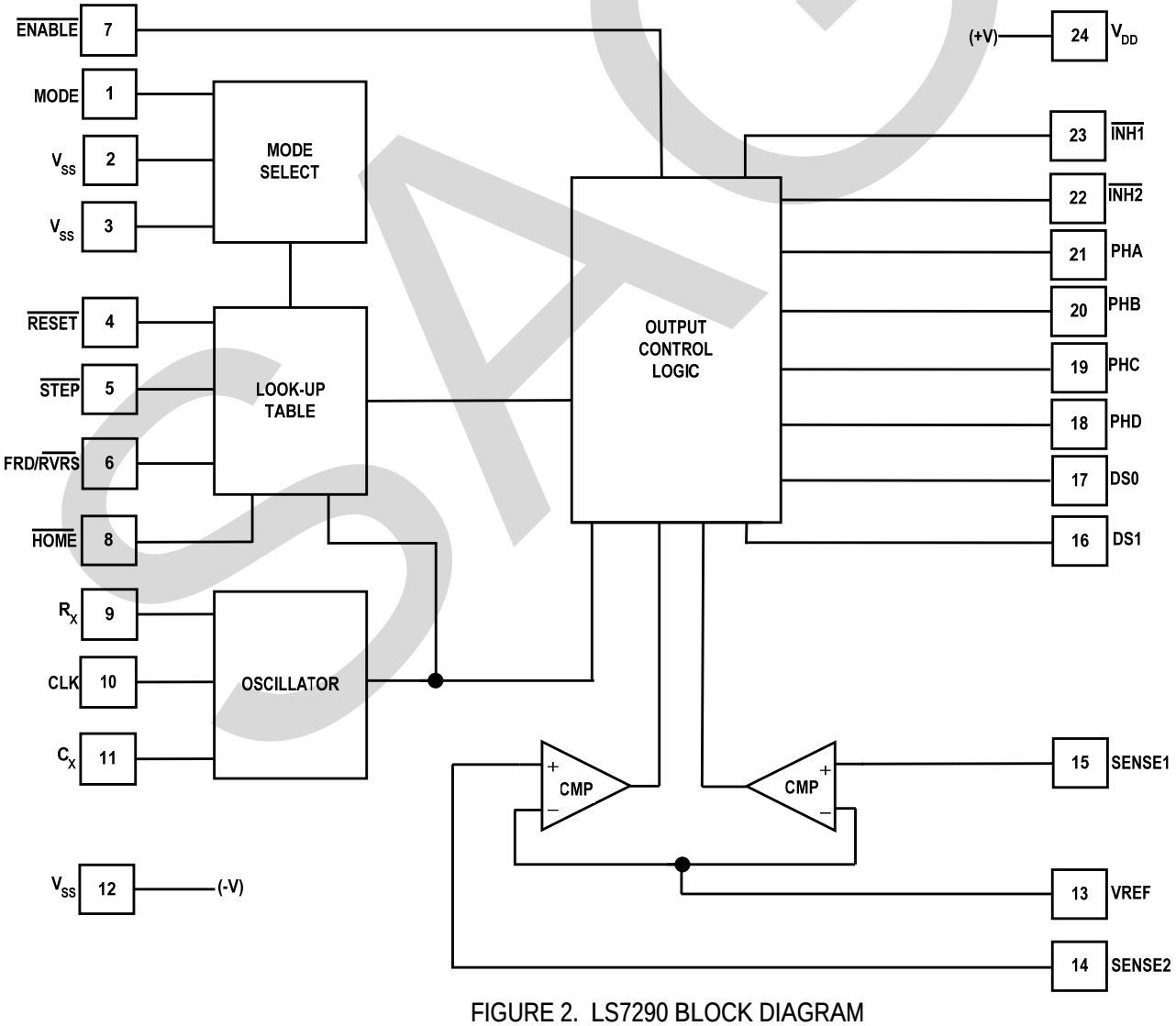


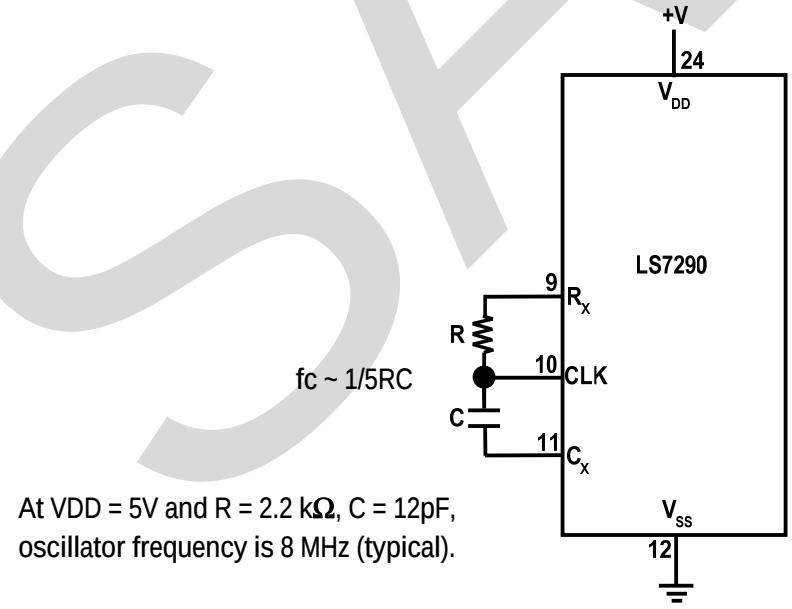
FIGURE 2. LS7290 BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} - V_{SS}	+7	V
Any Input Voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-20 to +85	°C
Storage Temperature	T_{STG}	-85 to +150	°C

ELECTRICAL SPECIFICATIONS (-25°C < T_A < +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	3.0	-	5.5	V	-
Supply Current	I_{DD}	-	-	2.0	mA	Outputs floating, Inputs high
CLK frequency	f_c		8.0	-	MHz	-
Enable Propagation Delay	t_{epd}	100	-	-	ns	-
FRD/RVRS Setup Time (before step pulse)	t_{ds}	0	-	-	µs	-
Step Pulse Width	SPW	1.0	-	-	µs	at f_c = 8 MHz
Interstep Pulse Delay	ISD	32	-	-	µs	at f_c = 8 MHz
Interstep Phase Blanking	IPB	1.25	-	5.0	µs	at f_c = 8 MHz
Reset Pulse Width	R_{PW}	1.0	-	-	µs	at f_c = 8 MHz
Reset to Step Pulse Delay	t_{rs}	0	-	-	µs	-
Hi-Level Input Voltage	V_{IH}	2	-	-	V	V_{DD} = 5 ± 0.25V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V	V_{DD} = 5 ± 0.25V
High-Level Input Current	I_H	-	-	50	nA	Leakage Current
Low-Level Input Current	I_L	-	-	50	nA	Leakage Current
Output Sink Current	I_O	-10	-	-	mA	V_O = 0.4V, V_{DD} = 5V
	I_O	-5	-	-	mA	V_O = 0.4V, V_{DD} = 3.3V
Output Source Current	I_O	5	-	-	mA	V_O = 4V, V_{DD} = 5V
	I_O	2.5	-	-	mA	V_O = 2.5V, V_{DD} = 3.3V
Comparator Offset Voltage	V_{OS}	-	5	15	mV	V_{REF} = 1V
Input Reference Voltage	V_{REF}	0.5	-	3.0	V	V_{DD} = 5V
	V_{REF}	0.5	-	1.5	V	V_{DD} = 3.3V



At VDD = 5V and R = 2.2 kΩ, C = 12pF, oscillator frequency is 8 MHz (typical).

FIGURE 3. RC OSCILLATOR FOR CLOCK GENERATOR

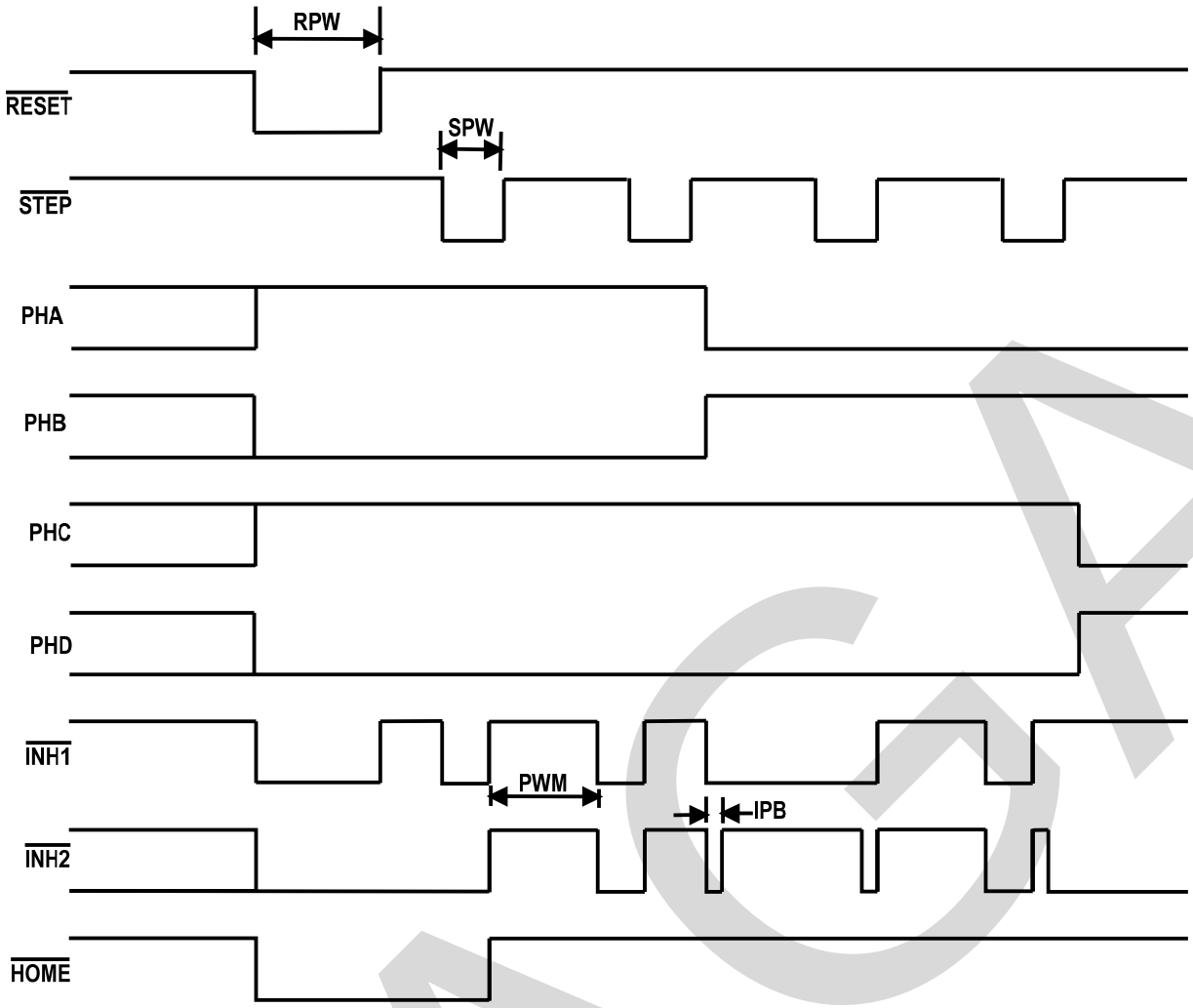


FIGURE 4. PARTIAL SEQUENCE IN FORWARD HALF- STEP MODE

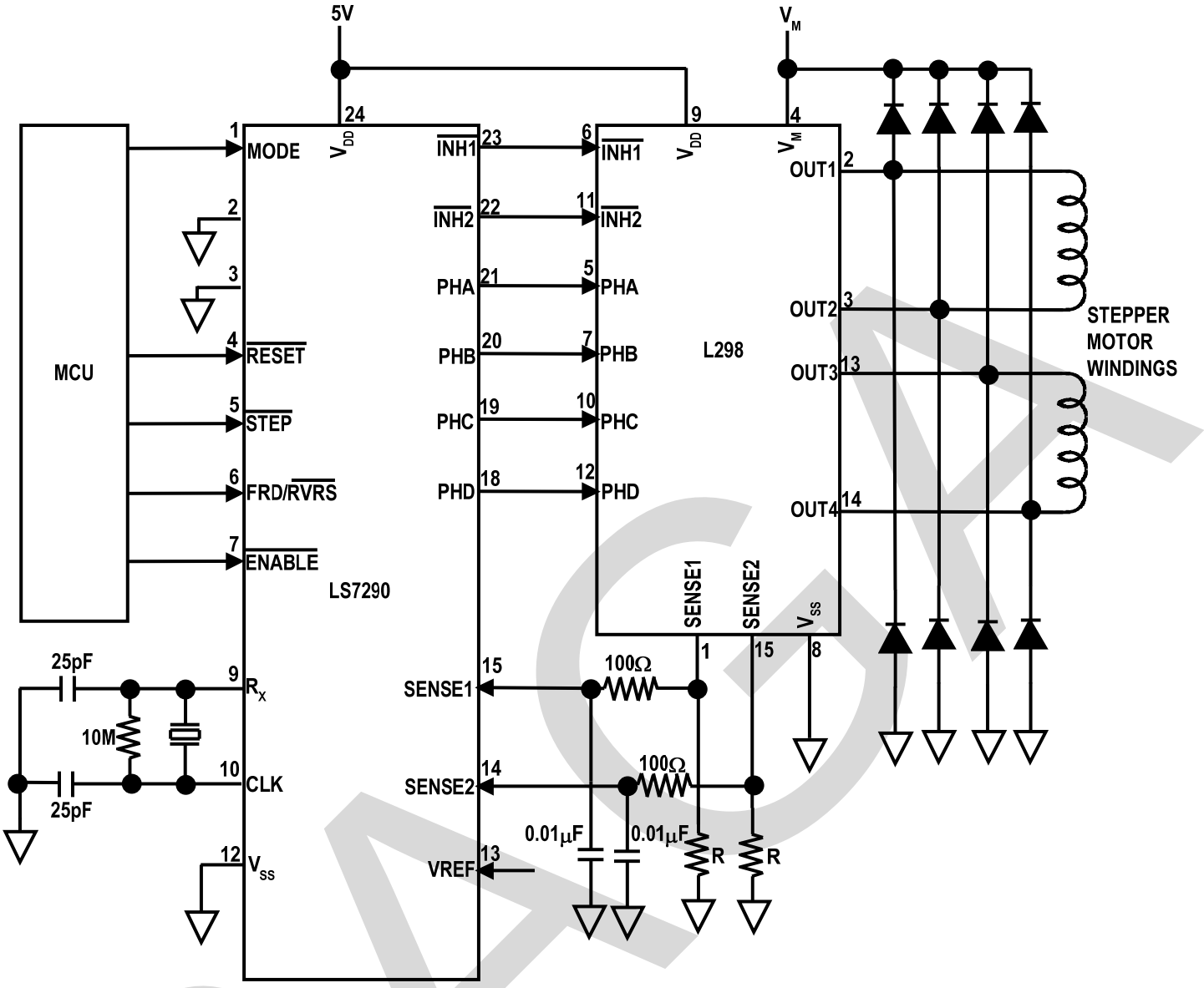


FIGURE 5. TYPICAL APPLICATION SCHEMATIC FOR A TWO PHASE BIPOLAR MOTOR USING A SINGLE MOTOR IC

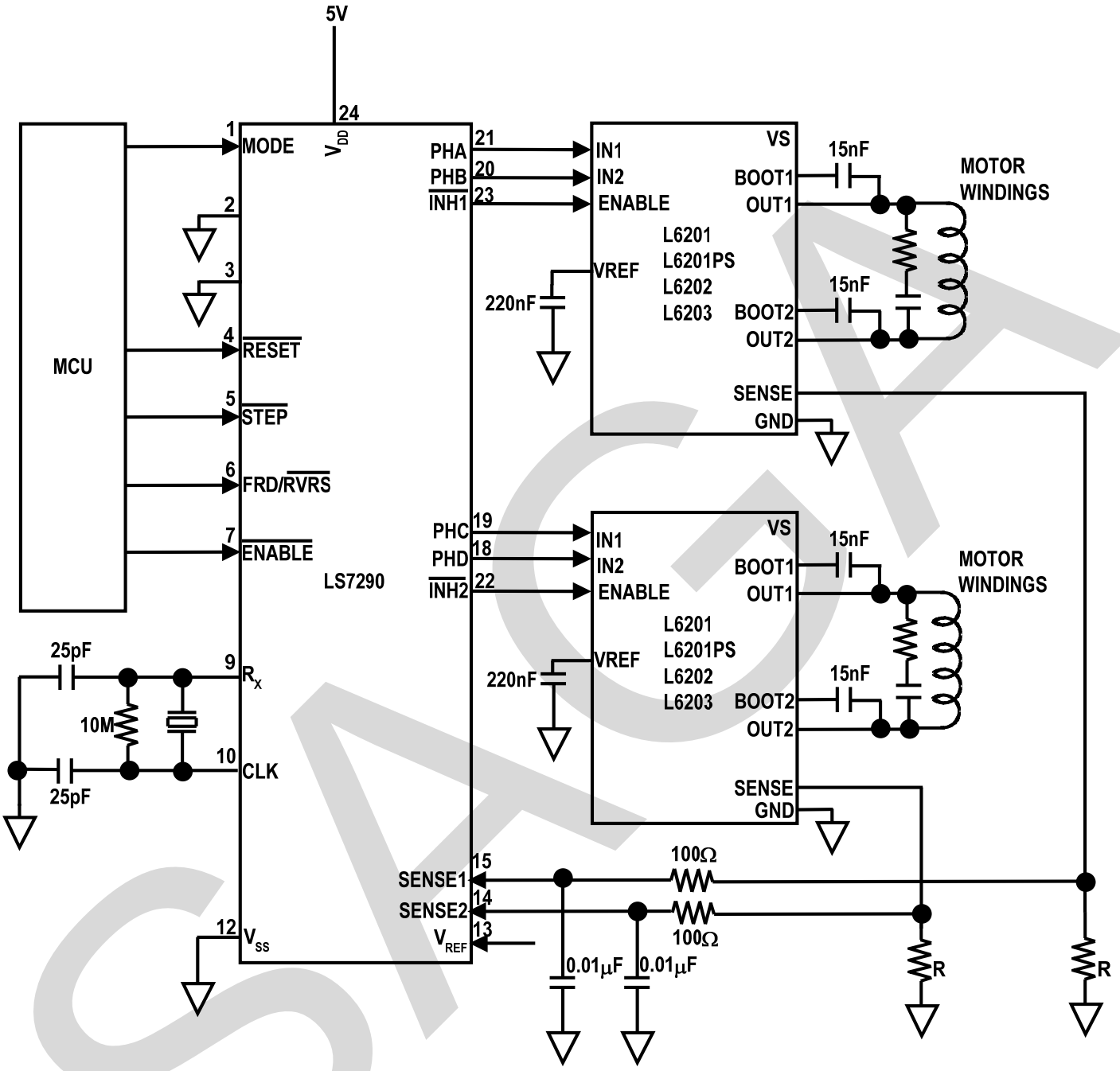
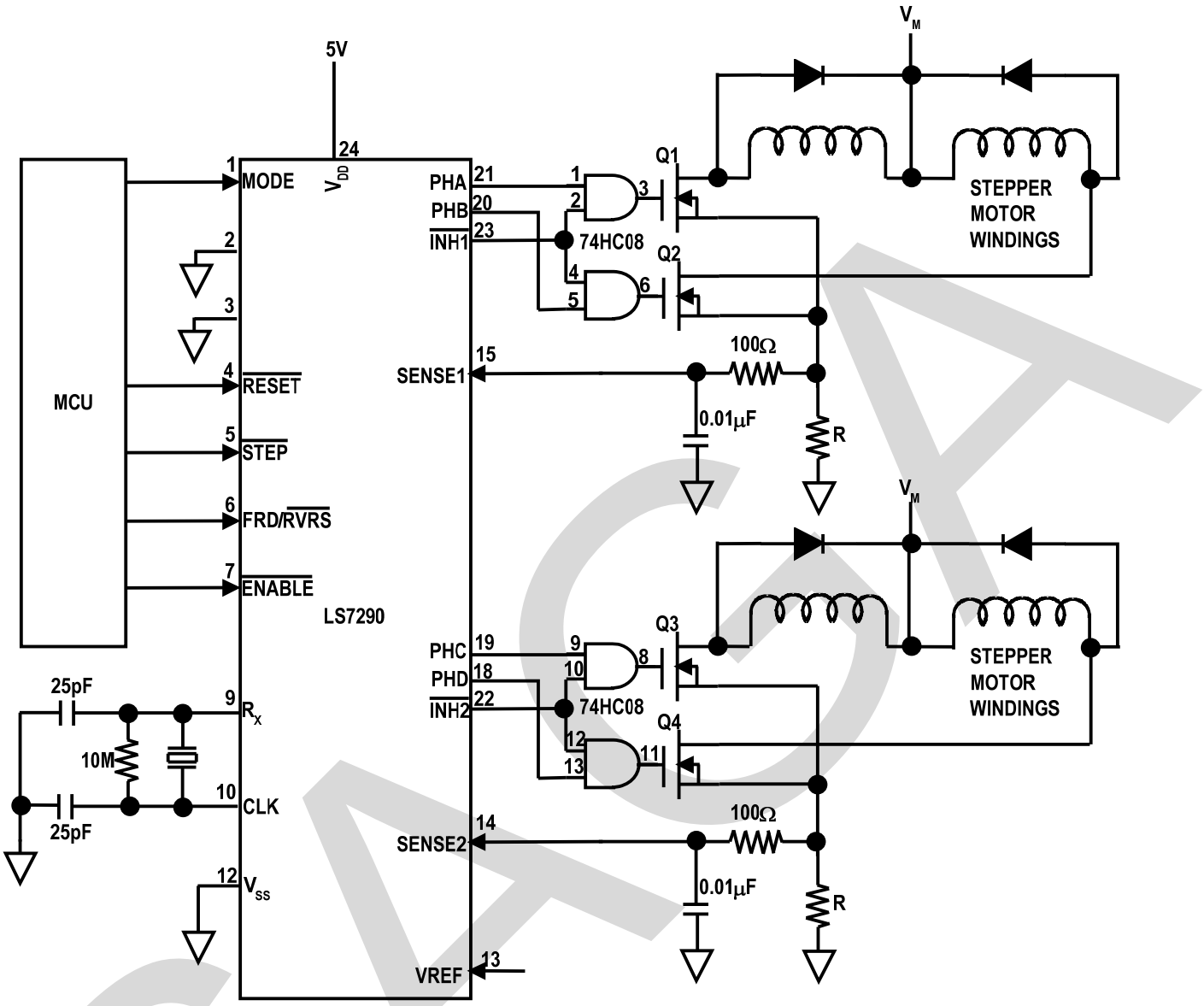


FIGURE 6. TYPICAL APPLICATION SCHEMATIC FOR A TWO PHASE BIPOLAR MOTOR USING TWO SEPARATE MOTOR DRIVER ICs



NOTE: Q1, Q2, Q3, Q4 are MOSFET Power Transistors suitable for 5V Gate Drive
Typical P/Ns = IRLZ44N and IRF3708

FIGURE 7. TYPICAL APPLICATION SCHEMATIC FOR A FOUR PHASE UNIPOLAR MOTOR USING DISCRETE MOSFET TRANSISTORS

TABLE 2								
STEP NUMBER		% DUTY CYCLE		PHASES				STEP ANGLE
FULL	1/2	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	
0	0	100	0	1	0	1	0	HOME
	1	70.7	70.7	1	0	1	0	45
1	2	0	100	0	1	1	0	90
	3	-70.7	70.7	0	1	1	0	135
2	4	-100	0	0	1	0	1	180
	5	-70.7	-70.7	0	1	0	1	225
3	6	0	-100	1	0	0	1	270
	7	70.7	-70.7	1	0	0	1	315
0	0	100	0	1	0	1	0	HOME

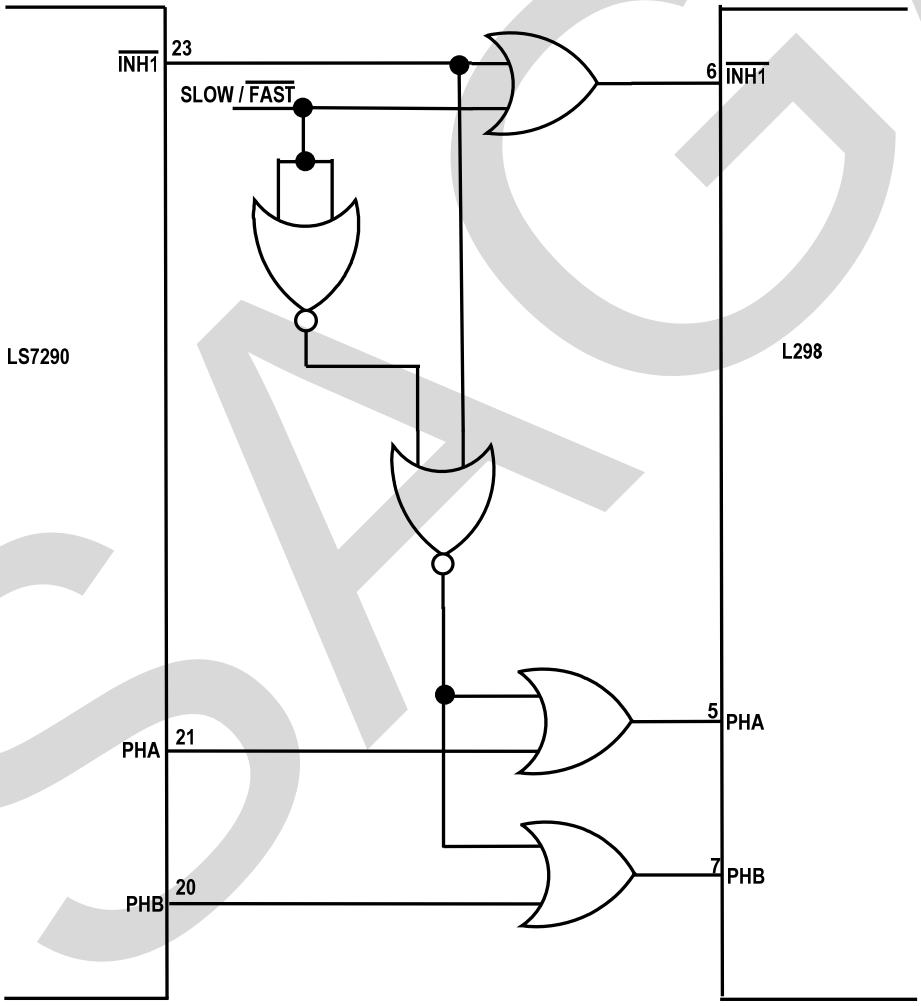
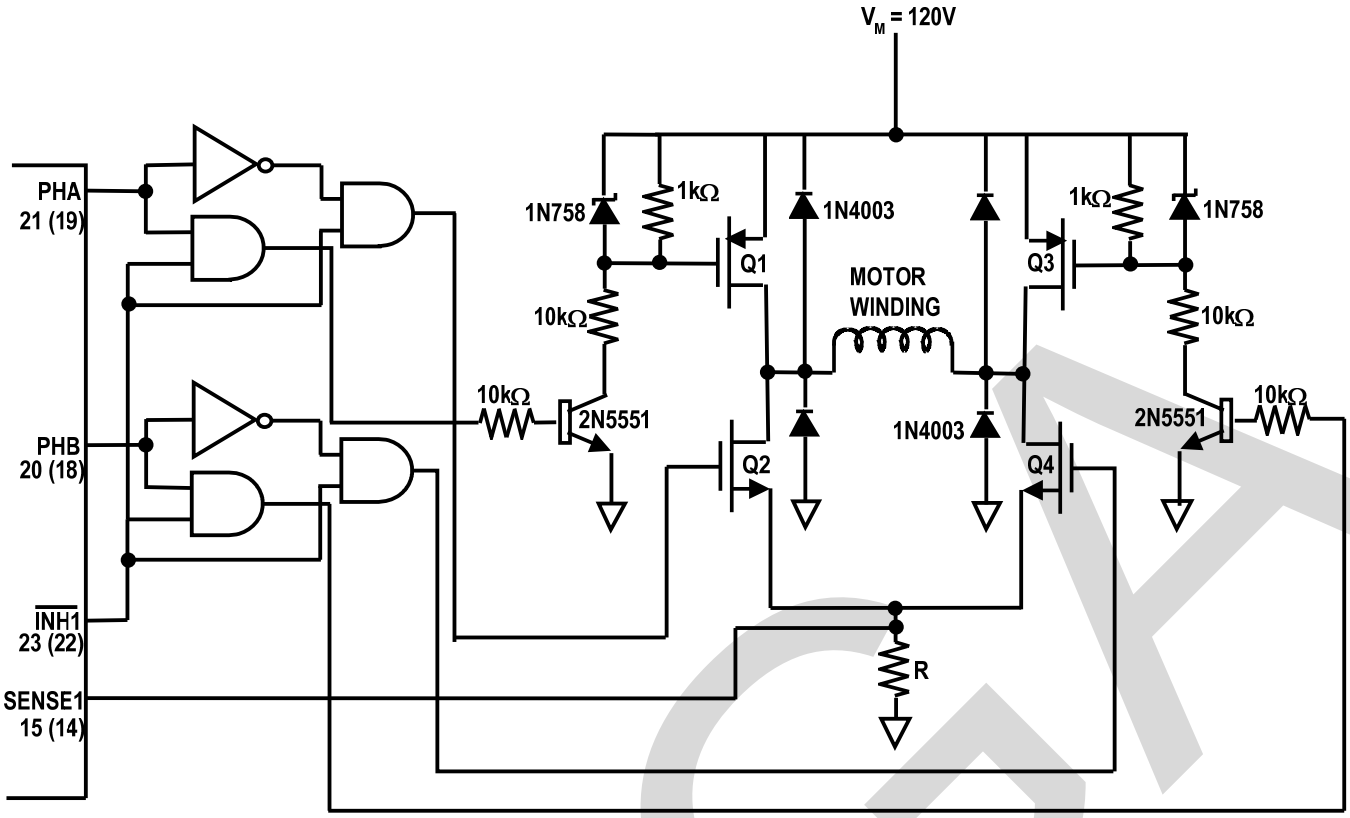


FIGURE 8. Selecting Between Fast and Slow Decay for One Stepper Motor Winding
(Use identical circuit for the other stepper motor winding)

NOTE: In fast decay mode, inhibit windings are chopped.
In slow decay mode, phase windings are chopped.

NOR Gates: CD4001 OR Gates: CD4071



Z = 10V
Inverters = 74HC04
Gates = 74HC08
Q1 = Q3 = IRF6215 (Typical)
Q2 = Q4 = IRLI3615 (Typical)

FIGURE 9. 120V Motor Discrete Component Driver